The VDTT M.TECH Programme

The VLSI Design, Tools, and Technology (VDTT) M.Tech. program at IIT Delhi is one of the most sought after Masters programmes in the country. It is one of the few programmes worldwide that only admit students sponsored by an industry or a research project. Each student has a co-supervisor from the sponsor and can do half of the final year project at the sponsor’s site. Typical GATE cutoffs for the admission interview have been in the 99.5 percentile or higher range.

Students in the programme choose one of three streams. The first is focused on analog and digital design; the second on machine learning and IoT; the last on sensors, devices, and nanotechnology.

VDTT students registering for placement have completed their core courses and need to take a few electives and complete their dissertation project. Many students have taped out custom ASICs and SOCs. The diversity of courses and the fact that these students form a very select band at the top of GATE examinees makes them a very sought after talent pool. Not only VLSI majors, but startups, leading analytics and computational finance organizations, and industries in the telecom sector have made offers to VDTT students in past years. Some VDTT students have started their own ventures, while others have done so after a few years.
Recruiting Excellence

Welcome to the VLSI Placement season of 2017 – 2018. As our students graduate into the VLSI industry, we believe they can contribute their best to this industry. This is because two years of course work and project work at IIT Delhi have equipped our students with the right skills, minds and attitudes to take on the pressures and demands of the corporate world.

The alumni of the VLSI group at IIT Delhi have been leaders and pioneers in academia and industry alike and we believe that the graduating students of the 2017-18 batch, will be no different in their commitment towards excellence. I am sure your organization will provide them the necessary incentives and motivation to continue to excel, even as they add to your technical strength and diversity.

We invite you to be a part of the placement season this year. We are sure this will be fruitful for our students as well as productive for your organization. We look forward to your active participation and hope that this will in turn strengthen the relationship that we as an institution enjoy with you.

Dr. Mukul Sarkar
Electrical Engineering Department
Coordinator of IEC Program
VLSI @ IIT Delhi

The VLSI group at IIT Delhi has been one of the oldest and most prominent groups in this field in India. Since its inception in the year 1976 the group has been actively involved in research and development with numerous publications, patents and tape-outs to its credit.


The VLSI group consists of distinguished faculty in this field renowned for their contributions through papers published in reputed journals and conference proceedings, book publications, guest lectures at various universities and conferences around the world and many other national and international awards. Many of them are associated with the editorial boards of leading journals and have consistently been part of the program committees of International Conferences in the VLSI domain.

The Doctoral and Masters Level students are handpicked from a narrowed down list of bright young students from all over India. The Professors also work very closely with many of the leading industries and research institutes in the country and work on research problems in collaboration with these organizations. This gives the students an opportunity to work on current issues pertaining to this field.
Courses

Program Core
- MOS VLSI design

Program Electives
- Advanced Data Structures
- Flexible Electronics
- Introduction to MEMS Design
- Photovoltaics
- Quantum Electronics
- Biomedical Electronics
- Active and Passive Filter Design
- Issues in Deep Submicron VLSI Design
- CAD for VLSI, MEMS, and Nanoassembly
- CMOS RF IC Design
- Embedded Intelligence
- Special Module in Low Power IC Design
- Special Module in VLSI Testing
- Numerical Optimization
- Architectures and Algorithms for DSP Systems
- CAD of RF and Microwave Circuits
- RF and Microwave Active Circuits

ASIC and SoC Design
- Synthesis of Digital Systems
- System Level Design and Modelling
- Digital System Design Laboratory
- Mixed Signal Circuit Design
- Analog Integrated Circuits
- Semiconductor Memory Design

Micro and Nano Devices
- I.C. Technology
- Micro and Nanoelectronics
- Micro and Nano Photonics
- Advanced Semiconductor Devices
- Compact Modeling of Semiconductor Devices
- Electronic and Photonic Nanomaterial

Embedded Intelligent Systems
- Advanced Topics in Embedded Computing
- Reconfigurable Computing
- Advanced Digital Signal Processing
- Neuromorphic Engineering
- Introduction to Machine Learning
- Energy-Efficient Computing
Resources

Laboratories
- VLSI Design Lab (EE)
- VLSI Design Lab (CSE)
- Digital Hardware Design Lab
- Data Analytics and Machine Learning Lab
- VDTT Lab

Tools and Design Software
- Cadence Design suite
- Synopsys Synthesis Tools
- Mentor Graphics Catapult C Synthesis
- Mentor Graphics IC Nanometer Design Tools
- MAGMA Physical Design Tools
- ATLAS device simulation framework
- Xilinx Foundation Series

Library
- IITD Central Library
- VDTT Library

Fabrication Facilities
- IC Fabrication and Testing facility at the CARE for 3 micron technology

Past/Ongoing Industrial Collaborations/Projects
- Intel, Texas Instruments, STMicroelectronics, IBM, Freescale, EADS, Calypto Design Solutions, Cypress Semiconductors, NXP Semiconductors, Synopsys, SiRF, Philips Research Netherlands, National Semiconductors, Nokia Research Germany, Cadence Design Solution.
Placements Brochure

Projects Undertaken by Students as part of Academic Courses

1. RISC based 32-bit general purpose processor.
2. Low power 8Kb SRAM design in 90nm.
3. RTL implementation of Built in Self Test & Repair for 64Kb memory.
4. Low Output Impedance Variable Gain Amplifier.
5. Design of optimized time constrained scheduling algorithm.
6. Frequency synthesizer for Digital Storage Oscilloscope.
7. X band Voltage Controlled Oscillator.
8. Verification of AMBA bus model using System Verilog.
9. 900 MHz All Digital Phase Locked Loop.
10. Designing a pipe-lined MIPS simulator.
11. Intelligent usage of DSP48 hardmacro to implement FFT with optimized area and high performance.
12. Content Addressable Memory with 8b input, 32b output and 2K address locations in 90nm technology.
13. Power amplifier with PAE 30-40% at 2.4GHz.
14. Developing Support Vector Classification & Support Vector Regression in C, CUDA & on FPGA.
15. Extending Simplescalar simulator for a pipelined multi-issue architecture.
16. Design of 2.4 GHz frequency synthesizer.
18. Ant Colony Optimization based Distributed Router.
**Student Profile 2015 - 17 Batch**

An exhaustive profile of the students of the 2015-2017 batch is presented in the attached leaflet. Below is a broad overview of their interests and specializations.

![Number of Students](chart.png)

**Recruitment Process**

Companies that wish to participate in the recruitment at IIT Delhi will be required to indicate the profile, preferred skill set and approximate Cost To Company ([http://tnp.iitd.ac.in/](http://tnp.iitd.ac.in/)). Based on this information, all the participating companies will be given slots beginning from Dec 1st. Companies can choose to give a pre-placement presentation, based on which students will opt for a company of their choice. Companies will then be allowed to shortlist from the resumes of the interested students and conduct tests and interviews for these students. The procedure is left to the company’s choice. All facilities and logistics for the recruitment will be arranged by the students here at IIT Delhi. Please refer attached letter for complete procedure.
# Faculty Profile

## Department Of Electrical Engineering

<table>
<thead>
<tr>
<th>Faculty Name</th>
<th>Research Areas</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prof. (Mrs). B. Bhaumik</td>
<td>Analog, Mixed Signal Circuit Design, Biological Neural Networks.</td>
</tr>
<tr>
<td>Prof. M. Jagadesh Kumar</td>
<td>Device Modeling, Device Technology.</td>
</tr>
<tr>
<td>Prof. Jayadeva</td>
<td>Machine Learning, VLSI Design and CAD, Neuromorphic Engineering, Swarm Intelligence.</td>
</tr>
<tr>
<td>Dr. Shouri Chatterjee</td>
<td>Analog, Mixed Signal Circuit Design, Filter Design and theory.</td>
</tr>
<tr>
<td>Dr. Anuj Dhawan</td>
<td>Plasmonics, Photonic devices, Nanofabrication, Biosensors, Chemical Sensors.</td>
</tr>
<tr>
<td>Dr. Mukul Sarkar</td>
<td>Solid State Imaging, CMOS image sensors, Neuromorphic Imaging.</td>
</tr>
<tr>
<td>Dr. Abhisek Dixit</td>
<td>Logic CMOS device design, characterization, Compact device modeling.</td>
</tr>
<tr>
<td>Dr. Madhusudan Singh</td>
<td>Flexible electronics, photovoltaics, organic light-emitting diodes</td>
</tr>
<tr>
<td>Dr. Bhaskar Mitra</td>
<td>MEMS and Microfabrication, Microfluidics, Microplasmas, Gas Phase Nanofluidics.</td>
</tr>
<tr>
<td>Dr. Manan Suri</td>
<td>Emerging Non-Volatile Memory Technology, Bio-inspired/Neuromorphic Computing</td>
</tr>
<tr>
<td>Dr. Debanjan Bhowmik</td>
<td>Magnetism, Spintronics, Micromagnetics, Memory devices, Condensed Matter Physics.</td>
</tr>
</tbody>
</table>
# Faculty Profile

## Department Of Computer Science and Engineering

<table>
<thead>
<tr>
<th>Name</th>
<th>Research Areas</th>
</tr>
</thead>
<tbody>
<tr>
<td>Prof. M. Balakrishnan</td>
<td>CAD for VLSI, Hardware-Software Co-design, Embedded Systems.</td>
</tr>
<tr>
<td>Prof. Anshul Kumar</td>
<td>CAD for VLSI, Computer Architecture, Embedded Systems.</td>
</tr>
<tr>
<td>Dr. Preeti R. Panda</td>
<td>System Modeling, Embedded Systems, Memory Synthesis, CAD for VLSI.</td>
</tr>
<tr>
<td>Dr. Kolin Paul</td>
<td>Reconfigurable Computing, FPGAs, Computer Architecture.</td>
</tr>
<tr>
<td>Dr. Smruti R. Sarangi</td>
<td>Computer Architecture, Operating Systems.</td>
</tr>
</tbody>
</table>

## Centre for Applied Research in Electronics

<table>
<thead>
<tr>
<th>Name</th>
<th>Research Areas</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dr. Samresh Das</td>
<td>Nanoelectronics and Optoelectronics.</td>
</tr>
<tr>
<td>Dr. Ankur Gupta</td>
<td>RF microelectronics, Nanotechnology and device circuit co-design.</td>
</tr>
<tr>
<td>Dr. Pushparaj Singh</td>
<td>Microelectromechanical systems (MEMS) sensors and Microelectronics.</td>
</tr>
</tbody>
</table>
# Past Recruiters

<table>
<thead>
<tr>
<th>Company Name</th>
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<tbody>
<tr>
<td>Intel</td>
<td>Qualcomm</td>
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<tr>
<td>NVIDIA</td>
<td>Rambus</td>
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<td>Cisco</td>
<td>Sequence Design</td>
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<td>Texas instruments</td>
<td>Maxim IC</td>
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<td>Magma</td>
<td>Mentor Graphics</td>
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<td>Synopsys</td>
<td>Synfora IEC</td>
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<tr>
<td>Analog Devices</td>
<td>Freescale Semiconductors</td>
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<td>IBM</td>
<td>Ikanos Communications</td>
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<tr>
<td>AMD</td>
<td>Juniper Networks</td>
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<tr>
<td>Cypress Semiconductors</td>
<td>Brocade</td>
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<tr>
<td>Cosmic Circuits</td>
<td>Sun Microsystems</td>
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<tr>
<td>NXP Semiconductors</td>
<td>Tejas Networks</td>
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<tr>
<td>Calyppto Design Systems</td>
<td>TANMIC</td>
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<tr>
<td>Nokia</td>
<td>Atrenta</td>
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<tr>
<td>Philips Research</td>
<td>Mechatronics</td>
</tr>
<tr>
<td>Apache Design Solutions</td>
<td>Aptina</td>
</tr>
<tr>
<td>ST Microelectronics</td>
<td></td>
</tr>
</tbody>
</table>
Training and Placement Cell

Dr. I. N. Kar
Professor-in-charge
Training and Placement Cell
IIT Delhi
hodtnp@admin.iitd.ac.in

Ms. Anishya Madan
Industrial Liaison Officer
Training and Placement Cell
IIT Delhi
placement@admin.iitd.ac.in

Professor-in-Charges

Prof. Jayadeva
Electrical Engineering Department
VDTT Program Coordinator

Dr. Mukul Sarkar
Electrical Engineering Department
IEC Program Coordinator

Dr. M. Veerachary
Electrical Engineering Department
Professor-in-charge
Training and Placement (Electrical)